What is Claimed is:

1. A split gate flash memory cell, comprising:

a substrate having a trench;

a conductive stud disposed in the lower trench and insulated from the substrate serving as a source line;

a source region formed in the substrate adjacent to the upper conductive stud;

an insulating layer disposed on the conductive stud;

a conductive spacer disposed on the upper sidewall of the trench serving as a floating gate, protruding and insulated from the substrate;

a first insulating stud disposed on the insulating layer, with the top thereof higher than that of the conductive spacer;

a first conductive layer disposed over the substrate of the outside conductive spacer serving as a control gate, the first conductive layer insulated from the conductive spacer and the substrate, respectively;

a first insulating spacer disposed on the sidewall of the insulating stud to cover the first conductive layer; and

a drain region formed in the substrate of the outside first conductive layer.

2. The memory cell as claimed in claim 1, further comprising a second conductive layer disposed between the first conductive layer and the first insulating spacer.

3. The memory cell as claimed in claim 2, wherein the second conductive layer is tungsten silicide.

4. The memory cell as claimed in claim 1, further comprising a second insulating spacer disposed on the sidewall of the first conductive layer.

5. The memory cell as claimed in claim 4, wherein the first and second insulating spacers are silicon nitride.

6. The memory cell as claimed in claim 1, further comprising:

a conductive plug disposed on the drain region serving as a bit line contact;

a cap layer disposed over the insulating stud and the first insulating spacer; and

a third conductive layer serving as a bit line disposed on the conductive plug and the cap layer.

7. The memory cell as claimed in claim 6, wherein the conductive plug is doped polysilicon.

8. The memory cell as claimed in claim 6, wherein the cap layer is silicon oxide.

9. The memory cell as claimed in claim 6, wherein the third conductive layer is tungsten.

10. The memory cell as claimed in claim 1, wherein the conductive stud is polysilicon.

11. The memory cell as claimed in claim 1, wherein the insulating layer is high density plasma oxide.

12. The memory cell as claimed in claim 1, wherein the conductive spacer is doped polysilicon.

13. The memory cell as claimed in claim 1, wherein the insulating stud is silicon oxide or boron silicate glass.

14. The memory cell as claimed in claim 1, wherein the first conductive layer is polysilicon.

15. A split gate flash memory cell, comprising:

a substrate having a trench;

a polysilicon stud disposed in the lower trench and insulated from the substrate serving as a source line;

a source region formed in the substrate adjacent to the upper polysilicon stud;

an insulating layer disposed on the polysilicon stud;

a polysilicon spacer disposed on the upper sidewall of the trench serving as a floating gate, protruding and insulated from the substrate;

an insulating stud disposed on the insulating layer, with the top thereof higher than that of the polysilicon spacer;

a polysilicon layer disposed over the substrate of the outside polysilicon spacer serving as a control gate, with the polysilicon layer insulated from the polysilicon spacer and the substrate, respectively;

a first insulating spacer disposed on the sidewall of the first insulating stud to cover the polysilicon layer;

a second insulating spacer disposed on the sidewall of the polysilicon layer; and

a drain region formed in the substrate of the outside polysilicon layer.

16. The memory cell as claimed in claim 15, further comprising a tungsten silicide layer disposed between the polysilicon layer and the first insulating spacer.

17. The memory cell as claimed in claim 15, wherein the first, second, and third insulating spacers are silicon nitride.

18. The memory cell as claimed in claim 15, further comprising:

a polysilicon plug disposed on the drain region serving as a bit line contact;

a cap layer disposed over the insulating stud and the first insulating spacer; and

a tungsten layer serving as a bit line disposed on the polysilicon plug and the cap layer.

19. The memory cell as claimed in claim 18, wherein the cap layer is silicon oxide.

20. The memory cell as claimed in claim 15, wherein the insulating layer is high density plasma oxide.

21. The memory cell as claimed in claim 15, wherein the first insulating stud is silicon oxide or boron silicate glass.